|  |
| --- |
|  logoPanchip Microelectronics Co., Ltd.**PAN5020****Datasheet****Video Processing SoC**Version: 1.0Release date: May 2019**Shanghai Panchip Microelectronics Co., Ltd.**Address: Room 802, No. 666 summerShanghai Zhangjiang Hi-Tech Park Road,People's Republic of ChinaTel: 021-50802371Website: <http://www.panchip.com> |

**USING THIS DOCUMENT**

The information in this document is subject to change without notice. Every effort has been made in the preparation of this document to ensure accuracy of the contents, but all statements, information, and recommendations in this document do not constitute a warranty of any kind, express or implied.

**TRADEMARKS**

Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

**DISCLAIMER**

All or part of the products, services and features described in this document may not be within the purchase scope or the usage scope. Unless otherwise specified in the contract, all statements, information, and recommendations in this document are provided "AS IS" without warranties, guarantees or representations of any kind, either express or implied.

**REVISION HISTORY**

|  |  |  |  |
| --- | --- | --- | --- |
| Version | Date | Description | Related Documents |
| v1.0 | May.2019 | Initial | - |

Contents

[Contents II](#_Toc10473267)

[Abbreviation V](#_Toc10473268)

[1 General Description 1](#_Toc10473269)

[1.1 Key Features 1](#_Toc10473270)

[1.2 Typical Applications 4](#_Toc10473271)

[2 Products List 5](#_Toc10473272)

[3 Block Diagram 6](#_Toc10473273)

[4 Pin Information 7](#_Toc10473274)

[4.1 QFN-56 Diagram 7](#_Toc10473275)

[4.2 QFN-56 Descriptions 8](#_Toc10473276)

[5 Reference Schematic Diagram 15](#_Toc10473277)

[6 Package Dimensions 16](#_Toc10473278)

[7 Precautions 17](#_Toc10473279)

[8 Storage Conditions 18](#_Toc10473280)

[9 Contact Us 19](#_Toc10473281)

**List of Figures**

[Figure 3‑1 PAN5020 Block Diagram 6](#_Toc10473262)

[Figure 4‑1 QFN56 Pin Diagram 7](#_Toc10473263)

[Figure 5‑1 Application Reference Circuit for QFN56 15](#_Toc10473264)

[Figure 6‑1 QFN56 Package Views 16](#_Toc10473265)

**List of Tables**

[Table 4‑1 QFN56 Pin Descriptions 8](#_Toc10473226)

[Table 6‑1 QFN56 Package Detail Parameters 16](#_Toc10473227)

Abbreviation

|  |  |
| --- | --- |
| ADC | Analog-to-Digital Converter |
| BOD | Brown-out Detector |
| DDR | Double Data Rate |
| DPLL | Digital PhaseLockedLoop |
| FPU | Floating-point Unit |
| GPIO | General-purpose Input/Output |
| I2C | Inter-Integrated Circuit |
| ISP | Image Signal Processor |
| LDO | Low Dropout Regulator |
| LVR | Low Voltage Reset |
| MCU | Microcontroller Unit |
| MPU | Memory Protection Unit |
| NVIC | Nested Vectored Interrupt Controller |
| PWM | Pulse Width Modulation |
| SIP | System-In-Package |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random Access Memory |
| UART | Universal Asynchronous Receiver/Transmitters |
| WDT | Watchdog Timer |
| WWDT | Window Watchdog Timer |

# General Description

The PAN5020 is a video processing SoC which has integrated 32-bit MCU, ISP, JPEG and H.264. The SOC is specially designed for accelerating video streaming performance, while H.264 encoder and JPEG encoder are mainly used for constructing the arts used in video streaming.

The MCU part of PAN5020 is the 32-bit microcontroller. It supports a wide range of applications from low-end, price sensitive designs to computing-intensive ones and provides advanced high-end features in economical products.

The PAN5020, which integrates with video encoder (H.264), JPEG codec, CMOS sensor interface, image sensor processor (ISP), ADC, can meet various kinds of application needs while save the BOM cost. The combination of DDR1, H.264 encoder, SDIO host controller makes the SOC the best choice for video streaming devices.

To reduce system complexity while cutting the BOM cost, the SOC also comes with a 56-pin SIP (System-In-Package) in QFN. The 64/128/256Mb DDR1 is stacked inside the SIP to ensure higher performance and minimize the system design efforts.

Moreover, the PAN5020 has many high-performance peripheral functions, such as general purpose I/O port with up to 41 pins, three 32-bit timers, four UARTs, two SPI interfaces, two I2C interfaces, one 16-bit PWM generators providing seven channels, an 6-channel 12-bit ADC, Watchdog Timer, Window Watchdog Timer, and a Brown-out Detector. All these peripherals have been incorporated into the PAN5020 to reduce component count, board space and system cost.

## Key Features

* **Core**
* MCU core running up to 200MHz with 4KB I-Cache & 16KB D-Cache
* Supports DSP extension with hardware divider
* Supports IEEE 754 compliant Floating-point Unit (FPU)
* Supports Memory Protection Unit (MPU)
* One 24-bit system timer
* Supports Low Power Sleep mode by WFI and WFE instructions
* Single-cycle 32-bit hardware multiplier
* Supports programmable 16 level priorities of Nested Vectored Interrupt Controller (NVIC)
* Supports programmable mask-able interrupts
* **Memory**
* 1024 KB Flash memory for program memory
* 8 KB SRAM for internal RAM (SRAM)
* 4K I-Cache used to cache instruction or literal data from SPI Flash
* 16K D-Cache used to cache data from DDR1
* 64/128/256Mb SDRAM with DDR1
* **Clock Control**
* Built-in 16MHz internal high speed RC oscillator (HIRC) for system operation
* Built-in 32 kHz internal low speed RC oscillator (LIRC) for lower power control
* Support external 16Mhz crystal
* 5 independent DPLLs for DDR/MCU/ISP/H264/Sensor
* **Video Input**
* Only support DVP interface, MIPI is not supported
* Support ITU-R BT 601/656 or RGB Bayer data
* Support 8/10/12-bit parallel input
* Pixel clock Configurable, max 84M
* Vsync/Hsync Configurable
* **ISP**
* Supports image size: (1920 x 1080), and any size from scaling down
* RGB Bayer demosaicing
* Black level compensation
* Defect pixel detection / correction
* Lens shade correction
* Filtering (noise, sharpness/blurring)
* Auto white balancing
* Auto exposure measurement
* Auto focus measurement
* Histogram calculation
* Color correction matrix
* Wide dynamic range
* Gamma correction
* Color space conversion to YCbCr
* Image scaling
* **H.264 Encoder**
* Supports ITU-T Recommendation H.264 Coding, Standard (MPEG-4 part 10) baseline profile Level 3.1 standard
* Supports up to the 720p+30w @50fps video resolution
* Supports YUV 4:2:0 video input format (MB base)
* Rate control
* Video stablization
* Encoder accelerate engine
* **JPEG Encoder**
* Baseline sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard supported.
* Support to encode interleaved YUV 4:2:2/4:2:0 and gray-level (Y only) format image
* **I/O Port**
* Up to 100Mhz
* Supports Push-Pull output, Open-Drain output, Input only with high impendence
* Schmitt trigger input
* **SDIO**
* Two master SDIO device
* Full compliance with SD Memory Card Specifications Version 2.0
* Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
* **Timer**
* Provides three channel 32-bit Timers; one 8-bit pre-scaler counter with 24-bit up-timer for each timer
* **WDT (Watchdog Timer)**
* Programmable clock source and time-out period
* Supports wake-up function in Power-down mode and Idle mode
* Interrupt or reset selectable on watchdog time-out
* **WWDT (Window Watchdog Timer)**
* 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible
* Supports 4-bit value (PSCSEL) to programmable maximum 11-bit prescale counter period of WWDT counter
* **PWM**
* One built-in 16-bit PWM generators, providing seven PWM outputs
* **UART (Universal Asynchronous Receiver/Transmitters)**
* Four UART devices
* Buffered receiver and transmitter, each with 168-byte FIFO
* **SPI (Serial Peripheral Interface)**
* Two SPI device
* Both Supports Master or Slave mode
* **I2C**
* Two I2C devices
* Supports Master/Slave mode
* Bidirectional data transfer between masters and slaves
* **ADC (Analog-to-Digital Converter)**
* Analog input voltage range: 0 ~ 2.4V or 0~1.4V
* 12-bit resolution
* Up to six single-end analog input channels
* Maximum ADC clock frequency is 24 MHz, and 14 ADC clocks per sample
* **BOD (Brown-out Detector)**
* With 4 programmable threshold levels: 3.0V/2.7V/2.4V/2.2V
* Supports Brown-out interrupt and reset option
* **LVR (Low Voltage Reset)**
* Threshold voltage level: 1.8±0.1V
* **Package**
* QFN56 package, 7 × 7 mm
* **DC/AC Charactaristics**
* Operating Temperature: -40℃~85℃
* Reliability: ESD HBM pass ±5KV
* Temperature sensor range: -20℃~140℃
* Power
* DPLL power 1.2V
* Digital core power 1.2V
* DDR power 2.4-2.7V
* General purpose IO power(SAVDD) 2.8-3.6V
* Camera Sensor IO power built in 1.8V or powered externally
* Power consumption
* Typical case: 720P@50FPS: 550mA

## Typical Applications

* Graphic transmission module

# Products List

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Name | FLASH(MB) | SDRAM(Mb) | I2C | SPI | UART | DMA |
| PAN5020A1AP | 1 | 64 | 2 | 2 | 4 | 1 |
| PAN2025A1BP | 1 | 128 | 2 | 2 | 4 | 1 |
| PAN2025A1CP | 1 | 256 | 2 | 2 | 4 | 1 |

# Block Diagram



Figure 3‑1 PAN5020 Block Diagram

# Pin Information

## QFN-56 Diagram

PAN5020 with QFN56 pin package pin-out is shown in Figure 4‑1.



Figure 4‑1 QFN56 Pin Diagram

## QFN-56 Descriptions

Detail pin descriptions see Table 4‑1.

Table 4‑1 QFN56 Pin Descriptions

|  |  |  |  |
| --- | --- | --- | --- |
| Pin Number | Pin Name | Pin Type | Description |
| 1 | P1.4 | I/O | General Purpose digital I/O pin |
| CMR\_D2 | DI | Camera D2 input pin |
| I2C0\_SDA | DI/DO | I2C0 data pin |
| I2S\_WS | DI | I2S WS pin |
| UART2\_RX | DI | UART2 RX pin |
| PWM3 | DO | PWM0 channel3 output pin |
| 2 | P1.3 | I/O | General Purpose digital I/O pin |
| CMR\_D3 | DI | Camera D3 input pin |
| I2C0\_SCL | DI/DO | I2C0 CLK pin |
| I2S\_CLK | DI | I2S CLK pin |
| UART2\_TX | DO | UART2 TX pin |
| PWM2 | DO | PWM0 channel2 output pin |
| 3 | P0.2 | I/O | General Purpose digital I/O pin |
| 4 | P0.1 | I/O | General Purpose digital I/O pin |
| 5 | P0.0 | I/O | General Purpose digital I/O pin |
| 6 | P1.2 | I/O | General Purpose digital I/O pin |
| CMR\_D4 | DI | Camera D4 input pin |
| SPI0\_MISO | DI/DO | SPI0 MISO pin |
| PWM1 | DO | PWM0 channel1 output pin |
| UART3\_RX | DI | UART3 RX pin |
| 7 | P1.1 | I/O | General Purpose digital I/O pin |
| CMR\_D5 | DI | Camera D5 input pin |
| SPI0\_MOSI | DI/DO | SPI0 MOSI pin |
| PWM0 | DO | PWM0 channel0 output pin |
| UART3\_TX | DO | UART3 TX pin |
| 8 | P1.0 | I/O | General Purpose digital I/O pin |
| CMR\_D6 | DI | Camera D6 input pin |
| SPI0\_CS | DO | SPI0 CS pin |
| UART3\_RTS | DO | UART3 RTS pin |
| 9 | P0.7 | I/O | General Purpose digital I/O pin |
| CMR\_D7 | DI | Camera D7 input pin |
| SPI0\_CLK | DI/DO | SPI0 CLK pin |
| UART3\_CTS | DI | UART3 CTS pin |
| 10 | P0.6 | I/O | General Purpose digital I/O pin |
| CMR\_D8 | DI | Camera D8 input pin |
| 11 | P0.5 | I/O | General Purpose digital I/O pin |
| CMR\_D9 | DI | Camera D9 input pin |
| 12 | VDD18\_Sensor | P | Power supply for sensor IO |
| 13 | SAVDD | P | Power supply |
| 14 | P4.3 | I/O | General Purpose digital I/O pin |
| UART1\_RTS | DO | UART1 RTS pin |
| UART0\_TX | DO | UART0 TX pin |
| SPI1\_MISO | DI/DO | SPI1 MISO pin |
| I2C1\_SDA | DI/DO | I2C1 data pin |
| SPI1\_CS | DI/DO | SPI1 CS pin |
| 15 | P4.5 | I/O | General Purpose digital I/O pin |
| UART0\_RX | DI | UART0 RX pin |
| I2C1\_SDA  | DI/DO | I2C1 data pin |
| SPI1\_CS | DI/DO | SPI1 CS pin |
| I2C1\_SCL | DI/DO | I2C1 CLK pin |
| SPI1\_MOSI | DI/DO | SPI1 MOSI pin |
| 16 | NRST | DI | Reset pin |
| 17 | DVDD\_DDR1 | P | DDR power supply |
| 18 | P4.6 | I/O | General Purpose digital I/O pin |
| ICE\_CLK | DI | ICE CLK pin |
| UART1\_RX | DI | UART1 RX pin |
| I2C0\_SCL | DI/DO | I2C0 CLK pin |
| SPI0\_CS | DI/DO | SPI0 CS pin |
| 19 | P4.7 | I/O | General Purpose digital I/O pin |
| ICE\_DAT | DI | ICE data pin |
| UART1\_TX | DO | UART1 TX pin |
| I2C0\_SDA | DI/DO | I2C0 data pin |
| SPI1\_CS | DI/DO | SPI1 CS pin |
| 20 | P5.6 | I/O | General Purpose digital I/O pin |
| ADC\_CH1 | AI | ADC channel1 analog input pin |
| I2S\_SD\_I | DI | I2S\_SD input pin |
| UART2\_RTS | DO | UART2 RTS pin |
| I2C0\_SDA | DI/DO | I2C0 data pin |
| I2C1\_SDA | DI/DO | I2C1 data pin |
| 21 | DVDD\_MCU1 | P | Digital core |
| 22 | P4.1 | I/O | General Purpose digital I/O pin |
| UART1\_RX | DI | UART1 RX pin |
| UART0\_CTS | DI | UART0 CTS pin |
| SPI1\_CS | DI/DO | SPI1 CS pin |
| I2C0\_SDA | DI/DO | I2C0 data pin |
| TM1\_IN | DI | TM1 input pin |
| SPI0\_MISO | DI/DO | SPI0 MISO pin |
| 23 | DVDD\_MCU2 | P | Digital core |
| 24 | SAVDD | P | Power supply |
| 25 | DVDD\_DDR2 | P | DDR power supply |
| 26 | P4.0 | I/O | General Purpose digital I/O pin |
| UART1\_TX | DO | UART1 TX pin |
| UART0\_RTS | DO | UART0 RTS pin |
| SPI1\_CLK | DI/DO | SPI1 CLK pin |
| I2C0\_SCL | DI/DO | I2C0 CLK pin |
| TM0\_IN | DI | TM0 input pin |
| SPI0\_MOSI | DI/DO | SPI0 MOSI pin |
| 27 | P5.4 | I/O | General Purpose digital I/O pin |
| I2C0\_SDA | DI/DO | I2C0 data pin |
| Flash\_CS | DO | Flash CS pin |
| I2S\_WS | DO | I2S WS pin |
| UART2\_RX | DI | UART2 RX pin |
| ADC\_CH5 | AI | ADC channel5 analog input pin |
| PWM3 | DO | PWM0 channel3 output pin |
| 28 | P5.3 | I/O | General Purpose digital I/O pin |
| I2C0\_SCL | DI/DO | I2C0 CLK pin |
| Flash\_SO | DI/DO | Flash SO pin |
| I2S\_CLK | DI | I2S CLK input pin |
| UART2\_TX | DO | UART2 TX pin |
| ADC\_CH4 | AI | ADC channel4 analog input pin |
| PWM2 | DO | PWM0 channel2 output pin |
| 29 | P5.2 | I/O | General Purpose digital I/O pin |
| I2C1\_SDA | DI/DO | I2C1 data pin |
| Flash\_WP | DI/DO | Flash WP pin |
| SPI0\_MISO | DI/DO | SPI0 MISO pin |
| PWM1 | DO | PWM0 channel1 output pin |
| UART3\_RX | DI | UART3 RX pin |
| SPI1\_MISO | DI/DO | SPI1 MISO pin |
| 30 | P5.1 | I/O | General Purpose digital I/O pin |
| I2C1\_SCL | DI/DO | I2C1 CLK pin |
| Flash\_HOLD | DI/DO | Flash HOLD pin |
| SPI0\_MOSI | DI/DO | SPI0 MOSI pin |
| PWM0 | DO | PWM0 channel0 output pin |
| UART3\_TX | DO | UART3 TX pin |
| SD0\_D3 | DI/DO | SD0 D3 pin |
| 31 | P5.5 | I/O | General Purpose digital I/O pin |
| ADC\_CH0 | AI | ADC channel0 analog input pin |
| I2S\_SD\_O | DO | I2S\_SD output pin |
| UART2\_CTS | DI | UART2 CTS pin |
| I2C0\_SCL | DI/DO | I2C0 CLK pin |
| I2C1\_SCL | DI/DO | I2C1 CLK pin |
| SD0\_D2 | DI/DO | SD0 D2 pin |
| 32 | P5.0 | I/O | General Purpose digital I/O pin |
| UART0\_RX | DI | UART0 RX pin |
| Flash\_SCLK | DO | Flash SCLK output pin |
| SPI0\_CS | DI/DO | SPI0 CS pin |
| ADC\_CH3 | AI | ADC channel3 analog input pin |
| UART3\_RTS | DO | UART3 RTS pin |
| SD0\_D1 | DI/DO | SD0 D1 pin |
| 33 | P3.7 | I/O | General Purpose digital I/O pin |
| UART0\_TX | DO | UART0 TX pin |
| Flash\_SI | DI/DO | Flsah SI pin |
| SPI0\_CLK | DI/DO | SPI0 CLK pin |
| ADC\_CH2 | AI | ADC channel2 analog input pin |
| UART3\_CTS | DI | UART3 CTS pin |
| SD0\_D0 | DI/DO | SD0 D0 pin |
| 34 | P3.3 | I/O | General Purpose digital I/O pin |
| SD0\_D0 | DI/DO | SD0 D0 pin |
| SD0\_CMD | DI/DO | SD0 CMD pin |
| 35 | P2.6 | I/O | General Purpose digital I/O pin |
| SD1\_D3 | DI/DO | SD1\_D3 pin |
| SPI1\_MOSI | DI/DO | SPI1 MOSI pin |
| PWM6 | DO | PWM0 channel6 output pin |
| I2S\_SD\_O | DO | I2S\_SD output pin |
| TM1\_CNT\_OUT | DO | TM1\_CNT output pin |
| SD0\_CLK | DO | SD0 CLK pin |
| 36 | P2.5 | I/O | General Purpose digital I/O pin |
| SD1\_D2 | DI/DO | SD1\_D2 pin |
| SPI1\_CS | DI/DO | SPI1 CS pin |
| PWM5 | DO | PWM0 channel5 output pin |
| I2S\_WS | DO | I2S WS pin |
| TM2\_CNT\_OUT | DO | TM2\_CNT output pin |
| SD1\_D3 | DI/DO | SD1 D3 pin |
| 37 | P3.1 | I/O | General Purpose digital I/O pin |
| SD0\_CMD | DI/DO | SD0 CMD pin |
| SD1\_D2 | DI/DO | SD1 D2 pin |
| 38 | P2.4 | I/O | General Purpose digital I/O pin |
| SD1\_D1 | DI/DO | SD1 D1 pin |
| SPI1\_CLK | DI/DO | SPI1 CLK pin |
| PWM4 | DO | PWM0 channel4 output pin |
| I2S\_CLK | DI | I2S CLK input pin |
| INT1 | DI | External interrupt pin1 |
| 39 | P3.0 | I/O | General Purpose digital I/O pin |
| SD0\_CLK | DO | SD0 CLK pin |
| SD1\_D0 | DI/DO | SD1 D0 pin |
| 40 | P2.3 | I/O | General Purpose digital I/O pin |
| SD1\_D0 | DI/DO | SD1 D0 pin |
| SPI0\_MISO | DI/DO | SPI0 MISO pin |
| PWM3 | DO | PWM0 channel3 output pin |
| I2C1\_SDA | DI/DO | I2C1 data pin |
| INT0 | DI | External interrupt pin0 |
| SD1\_CMD | DI/DO | SD1 CMD pin |
| 41 | P3.6 | I/O | General Purpose digital I/O pin |
| SD0\_D3 | DI/DO | SD0 D3 pin |
| SD1\_CLK | DO | SD1 CLK output pin |
| 42 | P2.2 | I/O | General Purpose digital I/O pin |
| SD1\_DET | DI | SD1\_DET pin |
| SPI0\_MOSI | DI/DO | SPI0 MOSI pin |
| PWM2 | DO | PWM0 channel2 output pin |
| I2C1\_SCL | DI/DO | I2C1 CLK pin |
| TM2\_IN | DI | TM2 input pin |
| 43 | XC2 | AO | Crystal pin2 |
| 44 | XC1 | AI | Crystal pin1 |
| 45 | P2.1 | I/O | General Purpose digital I/O pin |
| SD1\_CMD | DI/DO | SD1 CMD pin |
| SPI0\_CS | I/O | SPI0 CS pin |
| PWM1 | O | PWM0 channel1 output pin |
| I2C0\_SDA | I/O | I2C0 data pin |
| TM1\_IN | DI | TM1 input pin |
| UART0\_RX | DI | UART0 RX pin |
| 46 | DVDD\_DDR3 | P | DDR power supply |
| 47 | P2.0 | I/O | General Purpose digital I/O pin |
| SD1\_CLK | DO | SD1 CLK output pin |
| SPI0\_CLK | DI/DO | SPI0 CLK pin |
| PWM0 | DO | PWM0 channel0 output pin |
| I2C0\_SCL | DI/DO | I2C0 CLK pin |
| TM0\_IN | DI | TM0 input pin |
| UART0\_TX | DO | UART0 TX pin |
| 48 | DVDD\_MCU3 | P | Digital core |
| 49 | P3.5 | I/O | General Purpose digital I/O pin |
| I2C1\_SCL | DI/DO | I2C1 CLK pin |
| SD0\_D2 | DI/DO | SD0 D2 pin |
| UART3\_TX | DO | UART3 TX pin |
| SPI1\_CLK | DI/DO | SPI1 CLK pin |
| 50 | P3.4 | I/O | General Purpose digital I/O pin |
| SD0\_D1 | DI/DO | SD0 D1 pin |
| I2C0\_SCL | DI/DO | I2C0 CLK pin |
| I2C1\_SCL | DI/DO | I2C1 CLK pin |
| 51 | P1.6 | I/O | General Purpose digital I/O pin |
| CMR\_D0 | DI | Camera D0 input pin |
| I2S\_SD\_I | DI | I2S\_SD input pin |
| UART2\_RTS | DO | UART2 RTS pin |
| I2C0\_SDA | DI/DO | I2C0 data pin |
| I2C1\_SDA | DI/DO | I2C1 data pin |
| 52 | DVDD\_MCU4 | P | Digital core |
| 53 | SENSOR\_CLKO | O | Sensor clock output pin |
| 54 | P0.4 | I/O | General Purpose digital I/O pin |
| CMR\_D10 | DI | Camera D10 input pin |
| 55 | DVDD\_DDR4 | P | DDR power supply |
| 56 | P0.3 | I/O | General Purpose digital I/O pin |
| CMR\_D11 | DI | Camera D11 input pin |

# Reference Schematic Diagram



Figure 5‑1 Application Reference Circuit for QFN56

# Package Dimensions



Figure 6‑1 QFN56 Package Views

Table 6‑1 QFN56 Package Detail Parameters

|  |  |  |  |
| --- | --- | --- | --- |
|  DIMSYMBOL | MIN.(mm) | NOM.(mm) | MAX.(mm) |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | 0.20 REF |
| b | 0.15 | 0.20 | 0.25 |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| D2 | 5.05 | 5.20 | 5.35 |
| E2 | 5.05 | 5.20 | 5.35 |
| e | 0.30 | 0.40 | 0.50 |
| K | 0.20 | - | - |
| L | 0.35 | 0.40 | 0.45 |
| R | 0.09 | - | - |

# Precautions

1. This product is a CMOS device and should be protected against static electricity during storage, transportation and use.
2. Grounding when device is in use.
3. Reflow temperature can not exceed 260℃.

# Storage Conditions

1. Products should be stored in sealed packages: when the temperature is less than 30 degrees and the humidity is less than 90%, it can last for 12 months.
2. After the package is opened, the components will be used in the reflow process or other high-temperature processes. The following conditions must be met:
3. Completed within 72 hours and the factory environment is less than 30℃≤ 60% RH.
4. Stored in 10% RH environment.
5. Exhaust at 125℃ for 24 hours to remove internal water vapor before used.

# Contact Us

Shanhgai headquarters

Tel: 021-50802371

Fax: 021-50802372

Add:Room 802, No.666 summer, Shanghai Zhangjiang Hi-Tech Park Road

Suzhou R&D center

Tel: 0512-68136052

Fax: 0512-68136051

Add: 4th floor, Fuhua Technology Building, No.199 Chongwen Road, Suzhou, Jiangsu Province

Shenzhen Agency

Tel: 0755-26403799

Fax:0755-26403799

Add: Room 106, Weijie Building, Sangda Hi-tech Park No.11, Technology Road, Nanshan District